REMARKS

Claims 1-7 have been withdrawn from consideration.

Claims 8-10 have been rejected under 35 USC 103(a) as unpatentable over Henle in view of Kinsman. The rejection is respectfully traversed.

Henle discloses several semiconductor chips which are designed so that the signal and power terminals are brought to one edge of the integrated circuit chips. Henle discloses, in one embodiment, semiconductor chips 10 which are physically and electrically connected to a substrate 11 at one edge of the semiconductor chip 10. All signals and power terminals 12 of each semiconductor chip 10 are located on that one edge of the chip. Electrical conductors 13 are located on or in the substrate 11 to which the terminals 12 are connected. The semiconductor chips 10, however, do not comprise electrical lines printed on one of the main sides of the semiconductor chips 10. Additionally, no two semiconductor chips 10 are bonded together for producing a chip composite.

Henle fails to disclose adhesively bonding two semiconductor chips 10 together. Hence, there is no reason why the skilled artisan would have been motivated to use the semiconductor chips 10 to manufacture a chip composite or a method for producing semiconductor components according to the invention.

In a second embodiment, Henle discloses an integrated circuit chip 35 (col. 6, line 64 to col. 7, line 51). The semiconductor chip 35 is produced using a tape carrier 30. As disclosed in col. 7, lines 30 to 51, the input output leads 37 of the chip 35 on one edge of the integrated circuit chip is bent to a right angle as shown in figures 6D, 6E and 6F. From figure 6D to 6F, the leads 37 do not run onto base sides of the semiconductor chips 35. Furthermore, the individual integrated chips 35 are only attached to the carrier 30, no two integrated circuit chips 35 are adhesively bonded together to produce a chip composite. As a result, the integrated circuit chip 35 as disclosed by Henle would not have motivated the skilled person to arrive at a method for producing semiconductor components according to the invention.

Henle discloses a third embodiment of the semiconductor integrated circuit chip 50 at col. 7, line 52 to col. 8, line 43. The integrated circuit chips 50 are compression-bonded to a tape carrier 52, but no two chips 50 are adhesively bonded together. The carrier 52 has openings in which the individual integrated circuit chips 35 are attached. Input output leads 55 of the circuit chips do not run from contact points of the semiconductor chips beyond the lower edges of the main sides onto the base side of the semiconductor chips. Furthermore, only single chips 50 are attached to the carrier 52. No chip composite having two chips adhesively bonded together are disclosed by Henle.

As a result, Henle does not disclose "printing electrical lines on main sides of semiconductor chips such that the lines run from contact points of the semiconductor chips beyond lower edges of the main sides onto base sides of the semiconductor chips." Nor does Henle disclose "producing a chip composite by adhesively bonding together two semiconductor chips."

Kinsman discloses a vertically mountable semiconductor device including a plurality of bond pads disposed proximate to a single edge thereof. The semiconductor devices 10 comprise bond pads 12 which may be disposed on short distance from edge 16, or the lower edges may be flush with the edge. Bond pads, however, are not electrical lines. Thus, Kinsman does not disclose "printing electrical lines on main sides of semiconductor chips such that the lines run from contact points of the semiconductor chips beyond lower edges of the main sides onto base sides of the semiconductor chips."

Kinsman, at col. 1, lines 1 to 27, discloses a laminated module 50 which includes a plurality of adjacent semiconductor devices 10 that are bonded together with a layer of laminate 52. When mounted to carrier substrate 30, the laminated module 50 has greater structure stability than a vertically mounted semiconductor device. The laminated module 50, however, is not a chip composite according to the claimed invention. Additionally, more than two semiconductor devices 10 are laminated together, i.e. most of the semiconductor devices are laminated on both of their main sides. Therefore, it is impossible that electric lines are printed on main sides of semiconductor devices 10 such that the lines run from contact points of the semiconductor devices 10 beyond lower

edges of the main sides onto base sides of the semiconductor devices, because this would result in a short circuit.

Since the recited structure and method are not disclosed by the applied prior art (either alone or in combination), claims 8-10 are allowable.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no.543822002200. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: December 20, 2005

Respectfully submitted,

By _____

Kevin R. Spivak
Registration No.: 43,148
MORRISON & FOERSTER LLP
1650 Tysons Blvd, Suite 300
McLean, Virginia 22102
(703) 760-7762